* R M - 6 5 2 9 / 1 0 0 *

RM-6529

B. E. - II (Sem. IV) (IC) Examination

May / June – 2010

Digital Integrated Circuit

Time : **3** Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ B. E. - 2 (Sem. 4) (IC)

Name of the Subject :

☛ Digital Integrated Circuit

☛ Subject Code No. : 6 5 2 9 ☛ Section No. (1, 2,.....) : 1&2

Seat No. :

Student's Signature

(2) Answers to the **two** sections must be tied **separately**.

(3) Assume suitable data wherever necessary.

(4) Figures to the right indicate full marks.

(5) Attempt **all** questions.

SECTION - I

1 (a) Answer the following in brief. **10**

(i) Define Fanout **1**

(ii) State the disadvantage of DCTL logic Family. **1**

(iii) Fanout of the ECL gate is highest (state: true/false) **1**

(iv) Which logic family is used in an industrial environment where electrical noise level is high? **1**

(v) State True/False: DTL is faster than TTL. **1**

(vi) What is passive Pull up? **2**

(vii) Explain Propagation Delay. **2**

(viii) Among TTL and ECL which logic family has higher power dissipation? **1**

(b) Show the calculation for fanout for RTL NOR gate and state the effect of temperature on fan out. **10**

2 (a) Explain Schottky TTL. 8

(b) (i) Draw circuit diagram of single npn transistor inverter which requires one power supply. 7

(ii) Find out the value of R_c given that V_{cc} = 6V, V_{cc} (sat) – 0.2 V, I_c (sat) = 10 mA.

(iii) For operating at edge of saturation, find the value of Rb, Bf = 50, Vbe (sat) = 0.7V, Vih = 2V.

OR

(b) Explain voltage transfer charactertistics of ECL OR gate. 7

3 Attempt any **three** : 15

(i) Explain wired and connection for DTL logic circuit with necessary diagram.

(ii) Discuss propagation delay hazards with diagram.

(iii) Explain active pull up and passive pull up with necessary diagram.

(iv) Why negative power supply is used in ECL?

(v) Explain the basic configuration of 12L family.

SECTION - II

4 (a) Answer the following questions in brief:

(i) Explain example of sequential Access memory. 2

(ii) Draw NMOS NAND gate. 2

(iii) Why PMOS is slower compared to NMOS? 2

(iv) Explain function of Refresh Circuit. 2

(v) Match the following : 2

(a)	ROM	(i)	Programmable AND fix OR
(b)	PLA	(ii)	fix AND programmable OR
(c)	PAL	(iii)	Programmable AND programmable OR

(b) Explain CMOS-BJT and BJT-CMOS interfacing in detail. 10

5 (a) Draw and explain BICMOS inverter with Bleeder resistor. Explain the need of Bleeder resistor. 8

(b) Derive the equation of rise time for MOS gate. 8

OR

(b) Explain ROM multiplier for two 4 bit numbers. 8

6 Attempt any **two** : **14**

(a) Draw and explain functional block diagram of IC 62256.

(b) Comparison of various logic family.

(c) Explain six transistor static RAM cell.